

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT9015**

**Nine wide Schmitt trigger buffer/line driver**

Product specification  
Supersedes data of March 1988  
File under Integrated Circuits, IC06

December 1990

## Nine wide Schmitt trigger buffer/line driver

## 74HC/HCT9015

### FEATURES

- Schmitt trigger action on all data inputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

The 74HC/HCT9015 are nine wide Schmitt trigger buffer/line drivers with Schmitt trigger inputs. These inputs transform slowly changing input signals into sharply defined jitter-free output signals.

The “9015” is identical to the “9014” but has non-inverting inputs.

### GENERAL DESCRIPTION

The 74HC/HCT9015 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	12	13	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

### ORDERING INFORMATION

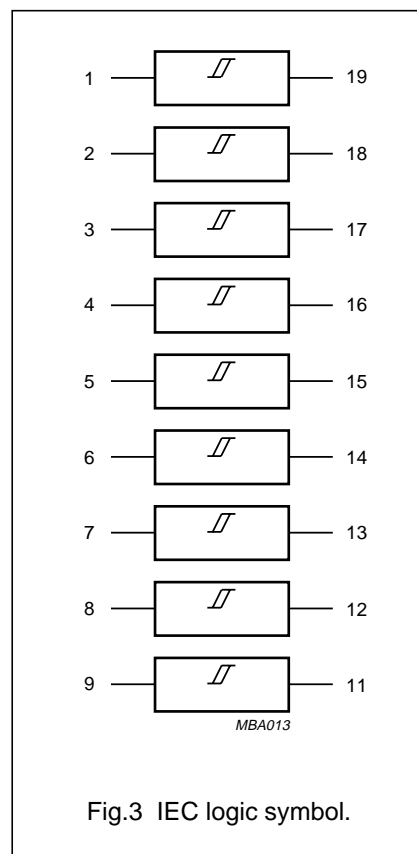
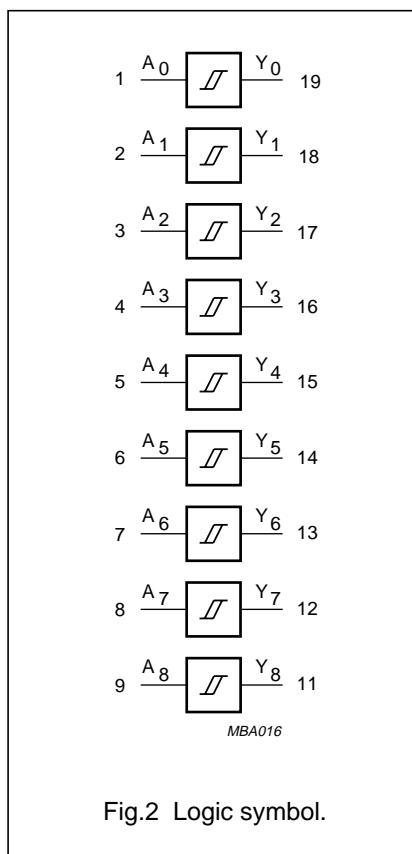
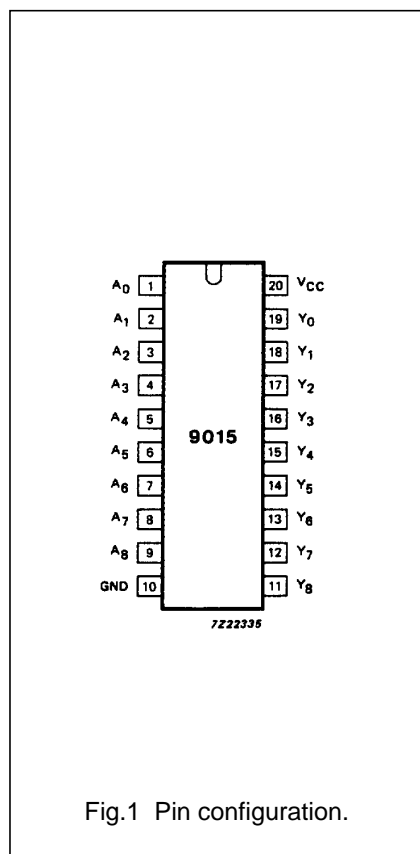
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

# Nine wide Schmitt trigger buffer/line driver

# 74HC/HCT9015

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9	A <sub>0</sub> to A <sub>8</sub>	data inputs
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12, 11	Y <sub>0</sub> to Y <sub>8</sub>	data outputs
20	V <sub>CC</sub>	positive supply voltage



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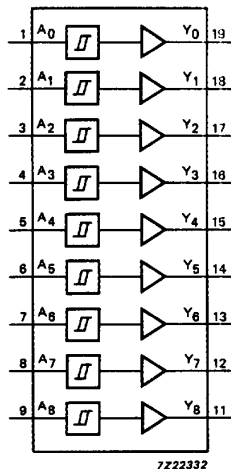


Fig.4 Functional diagram.

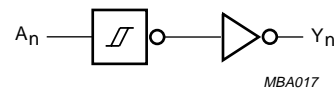


Fig.5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUTS	OUTPUTS
$A_n$	$Y_n$
L	L
H	H

Notes

1. H = HIGH voltage level  
L = LOW voltage level

## Nine wide Schmitt trigger buffer/line driver

## 74HC/HCT9015

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Transfer characteristics are given below.

Output capability: standard

I<sub>CC</sub> category: MSI

**TRANSFER CHARACTERISTICS FOR 74HC**

Voltages are referred to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HC									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V <sub>T+</sub>	positive-going threshold	0.70	1.13	1.50	0.70	1.50	0.70	1.50	V	2.0	Figs 6 and 7	
		1.75	2.37	3.15	1.75	3.15	1.75	3.15		4.5		
		2.30	3.11	4.20	2.30	4.20	2.30	4.20		6.0		
V <sub>T-</sub>	negative-going threshold	0.30	0.70	1.10	0.30	1.10	0.30	1.10	V	2.0	Figs 6 and 7	
		1.35	1.80	2.40	1.35	2.40	1.35	2.40		4.5		
		1.80	2.43	3.30	1.80	3.30	1.80	3.30		6.0		
V <sub>H</sub>	hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )	0.2	0.43	0.80	0.18	0.80	0.15	0.80	V	2.0	Fig.6	
		0.4	0.57	1.00	0.40	1.00	0.40	1.00		4.5		
		0.5	0.68	1.10	0.50	1.10	0.50	1.10		6.0		

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HC									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>		33	105		130		160	ns	2.0	Fig.8	
			12	21		26		32		4.5		
			10	18		22		27		6.0		
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19	75		95		110	ns	2.0	Fig.8	
			7	15		19		22		4.5		
			6	13		16		19		6.0		

## Nine wide Schmitt trigger buffer/line driver

## 74HC/HCT9015

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Transfer characteristics are given below.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A <sub>n</sub>	0.3

**TRANSFER CHARACTERISTICS FOR 74HCT**

Voltages are referred to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V <sub>T+</sub>	positive-going threshold	0.9 1.2	1.50 1.70	2.0 2.1	0.9 1.2	2.0 2.1	0.9 1.2	2.0 2.1	V	4.5 5.5	Figs 6 and 7	
V <sub>T-</sub>	negative-going threshold	0.7 0.8	1.06 1.27	1.4 1.7	0.7 0.8	1.4 1.7	0.7 0.8	1.4 2.7	V	4.5 5.5	Figs 6 and 7	
V <sub>H</sub>	hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )	0.2 0.2	0.44 0.44	0.8 0.8	0.2 0.2	0.8 0.8	0.2 0.2	0.8 0.8	V	4.5 5.5	Figs 6 and 7	

**AC CHARACTERISTICS FOR 74HCT**

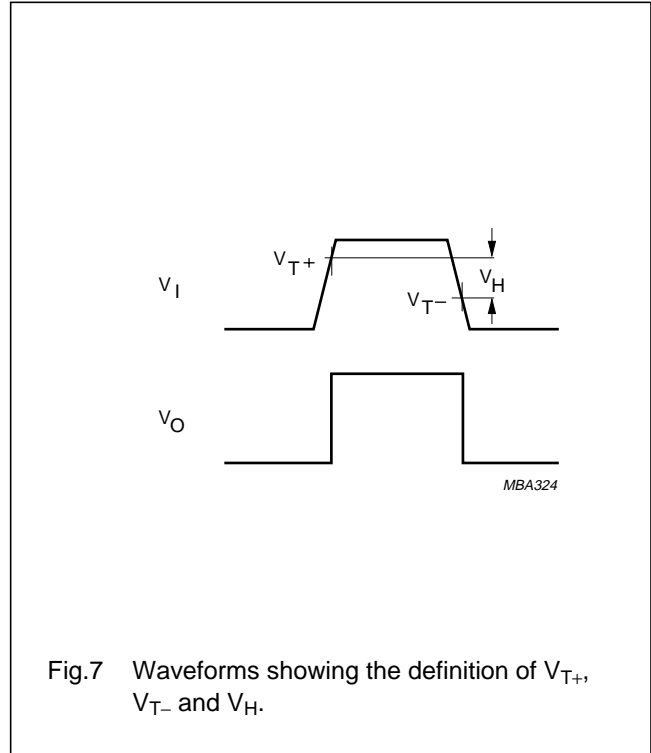
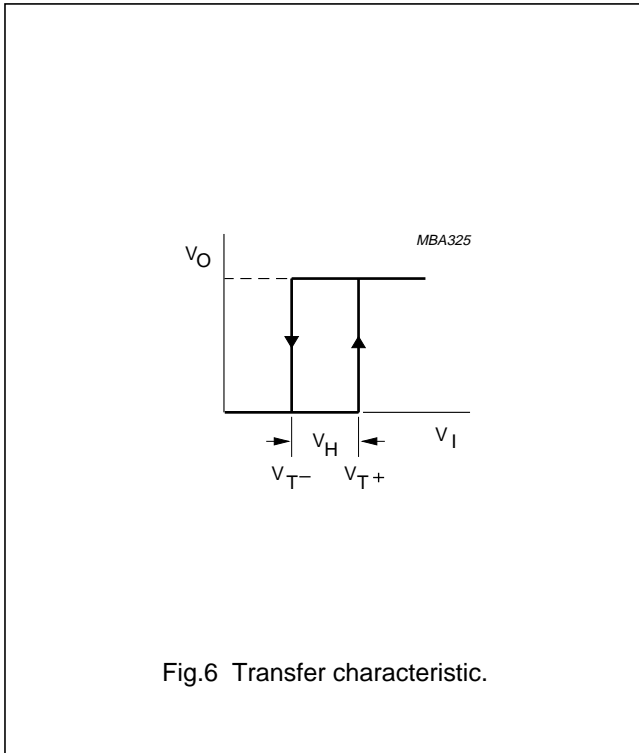
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>		18	32		40		48	ns	4.5	Fig.8	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.8	

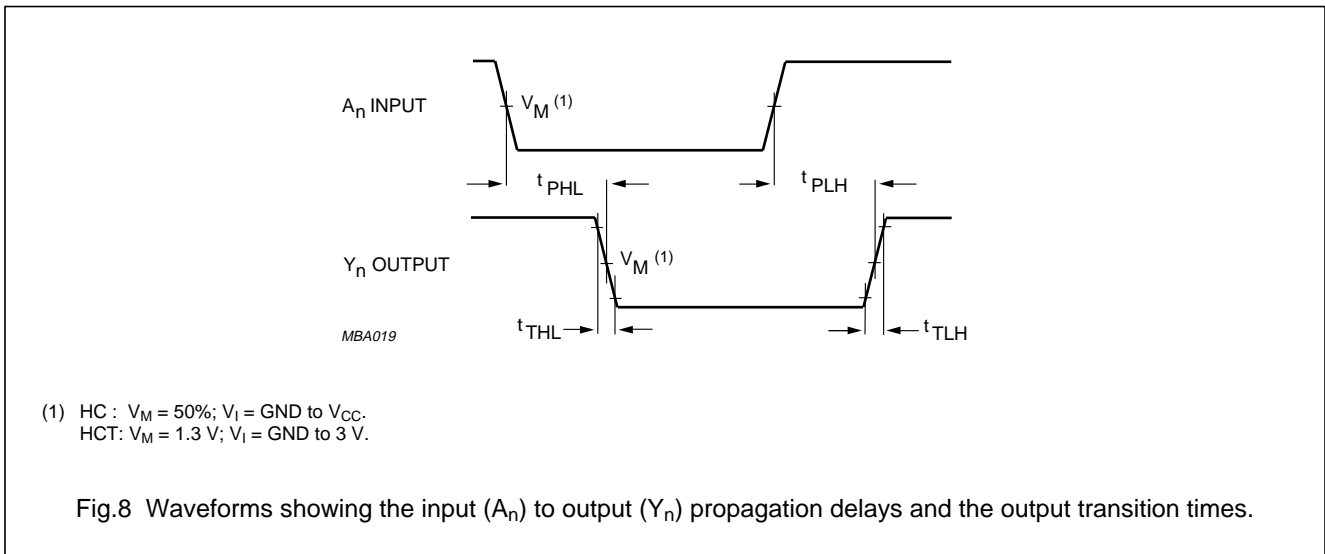
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TRANSFER CHARACTERISTIC WAVEFORMS



AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".